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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/029,829
Filing Date: December 27, 2001
Appellant(s): ZHONG ET AL.

Robert McDermott
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 7/12/07 appealing from the Office action mailed 11/15/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,197,087	IWAHASHI ET AL	3-1993
2001/0008544	ISHIYAMA	7-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-6, 8-15, and 17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwahashi et al (5,197,087).

Iwahashi et al, in Figures 1 and 3, discloses a signal encoding apparatus that is the same system and method for encoding a stream of data blocks using a scalable encoder as specified in claims 1-6, 8-15, and 17-21 of the present invention, the method comprising the steps of receiving a stream of data blocks 1; storing the received data blocks in a buffer (e.g. 11 or 12); encoding a first sequence of the stored data blocks from the buffer to produce a first encoded data block 17; monitoring the fullness level of the buffer (i.e. either utilizing ½ buffer length or the entire buffer) for comparison with a predetermined threshold range to yield an outcome of the comparison 15; and adjusting the complexity (e.g. 15, 16) of the encoder 17 based on the outcome.

With respect to claims 2-6, 8-15, and 17-21, Iwahashi et al also discloses the step of decreasing or increasing the complexity of the encoder when the fullness level of the buffer exceeds an upper limit or is below a lower level of the predetermined threshold range 15, respectively according to a predetermined encoding configuration table (e.g. DCT); encoding a second data block at the decreased or increased complexity to produce a second encoded data block 17; maintaining the complexity of the encoder when the fullness level of the buffer falls within the predetermined threshold range 16; wherein the fullness level of the buffer is determined based on an input rate of the stream of video frames 1.

Claims 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwahashi et al in view of Ishiyama (2001/0008544).

It is noted Iwahashi et al differs from the present invention in that it fails to particularly disclose any feed information from a memory as specified in claims 7 and 16. Ishiyama however, in Figures 1-8, teaches the concept of such well known storing of the encoded data blocks in a memory medium 40 for subsequent retrieval; and processing feedback information 105 from encoder 2 after producing the first encoded data block.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, having both the references of Iwahashi et al and Ishiyama before him/her, to incorporate the well known feedback technique as taught by Ishiyama in the encoding method of Iwahashi et al in order to accurately effect rate control.

(10) Response to Argument

Appellant argues that claim 1 specifies adjusting the complexity based on a comparison of a fullness of a buffer and a threshold. However, a recitation that "the adjustment is done based on a single buffer fullness level" is not found in Appellant's claim 1, as illustrated in Figure 1 of Appellant's Drawings. Without such specific limitation included in the claims, Examiner maintains that the invention of Iwahashi et al is consistent with Appellant's disclosure in its broadest sense where buffer fullness level may be either full or ½ full as an outcome during the adjustment of the encoding process.

One possible interpretation of Appellant's claim 1 requires a method of encoding video containing data blocks, comprising two steps:

(1) for one or more buffer fullness levels, encode the data blocks at a first complexity; and

(2) encode a different data block at a second complexity different from the first complexity.

Under this interpretation, Iwahashi et al discloses an encoder 17 for encoding one or more data blocks of a video stream in at least two different complexities (switch 16 opened or closed). The data blocks that are encoded when the switch is opened may be interpreted as only at half the complexity when compared to the data blocks that are encoded with the switch closed.

Another possible interpretation of Appellant's claim 1 that is also consistent with Appellant's Specification specifies a method of encoding data blocks of a video signal, comprising two processes:

(1) encode at least one data block of the video at a first complexity; and

(2) encode a second data block of the video at a second complexity greater than the first complexity.

Again, Figure 1 of Iwahashi et al also anticipates such alternative interpretation by disclosing two different encoding paths for performing two different processes. Based on the outcome of the energy comparisons (13, 14), encoder 17 encodes at least one data block of the video at a reduced complexity by adjusting the switch 16 to open through the block length determining circuit 15; and encoder 17 encodes at least one

other data block of the video at a complexity greater than the opened switch encoding processes by adjusting the switch 16 to close in order to encode the full buffer (11+12).

In conclusion, Examiner respectfully submits that Appellant's argument regarding independent claim 1 that the two different data blocks must be within a single buffer is not necessarily limited to Appellant's only interpretation.

Examiner acknowledges that Iwahashi et al may not describe a method identical to that disclosed by appellants. However, claims are to be given their broadest reasonable interpretation during prosecution, and the scope of a claim cannot be narrowed by reading disclosed limitations into the claim. See In re Morris, 127 F.3d 1048, 1054, 44 USPQ2D 1023, 1027 (Fed. Cir. 1997); In re Zletz, 893 F.2d 319, 321, 13 USPQ2D 1320, 1322 (Fed. Cir. 1989); In re Prater, 415 F.2d 1393, 1404, 162 USPQ 541, 550 (CCPA 1969). In addition, the law of anticipation does not require that a reference "teach" what an appellant's disclosure teaches. Assuming that reference is properly "prior art," it is only necessary that the claims "read on" something disclosed in the reference, i.e., all limitations of the claim are found in the reference, or "fully met" by it. Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Young Lee

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